Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A data processing device having Very Long Instruction Word (VLIW) architecture for processing VLIW instructions, the device comprising:

~~a~~ first and second functional ~~unit~~ units for performing one or more operations ~~having a relatively long latency~~ of an instruction at the same time, the first functional unit including a slave controller, ~~a second functional unit for performing~~ the one or more operations having a ~~relatively short~~ different latency; ~~, a common memory means shared by the first and second functional units,~~ and

a master controller for controlling a schedule for executing ~~an instruction~~ the one or more operations by the first functional unit~~, the execution of said instruction~~ including input/output operations that are performed by the slave controller of the first functional unit,

wherein said master controller synchronizes ~~at least one of output data of~~ the first functional unit to use output data processed by the second functional unit during the execution of said instruction ~~and the~~ to provide input data to ~~the first functional unit being generated by~~ the second functional unit during the execution of said instruction.

2. (Canceled)

3. (Previously presented) The data processing device according to claim 1, further comprising halt means controllable by the master controller for suspending operation of the first functional unit.

4. (Currently amended) A method of operating a data processing device having Very Long Instruction Word (VLIW) architecture for processing VLIW instructions, the method comprising acts of:

performing, at the same time, one or more operations of an instruction using a first functional unit, which includes a slave controller, ~~the first functional unit being arranged for executing operations having a relatively long latency,~~ and a second functional unit, ~~capable of executing~~ the one or more operations having ~~a relatively short~~ different latency;~~,~~ and

controlling with a master controller, ~~to control~~ a schedule for executing ~~an instruction~~ the one or more operations including input/output operations performed by the slave controller~~,~~ during execution of the instruction by the first functional unit; ~~receives input data and provides output data,~~ and

~~wherein~~ synchronizing with said master controller ~~synchronizes at least one of output data of~~ the first functional unit to use output data processed by the second functional unit during the execution of said instruction and ~~the~~ to provide input data to ~~the first functional unit being generated by~~ the second functional unit during the execution of said instruction.

5. (Previously presented) The method according to claim 4, further comprising an act of the master controller temporarily suspending operation of the first functional unit during execution of the instruction.